> The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It has not been adequately examined how the negative reactance component values are incorporated into existing reactive components that are not identified as negative since negative reactance is normally generated by active circuits.

(Office Action, p. 2.)

In addition, the Office Action categorizes U.S. Patent No. 6,285,251 to Dent et al. ("Dent"), as pertinent to applicant's disclosure. As stated in the Office Action, "Dent et al. Disclose a Chireix type amplifier in fig. 7 for instance including active switching amplifiers 312, 314 and output resonator 550 connected via combiner 320 that may be read as an impedance converter; however, Dent et al. do not address incorporating negative reactance values required into other existing reactive components." (Id.)

Applicants respectfully traverse the rejections set forth in the Office Action.

In relevant part, Dent discloses a distributed circuit which couples the outputs of two amplifiers in order to combine their output signals. Dent's circuit, illustrated in Fig. 7, comprises a distributed element layout which makes use of quarter wavelength transmission lines rather than inductors or capacitors. Specifically, Dent describes:

> the interactive coupler 320' that couples the first and second amplifiers 312 and 314 to the load impedance 326 is embodied by first and second quarter wavelength transmission lines 422 and 424 respectively. The load impedance includes an input node 440, and the first and second quarter wavelength transmission lines 422 and 424 are preferably coupled to the input node 440.

(Dent, column 11, lines 39-43).

Dent's interactive coupler 320' is physically large, being at least a quarter wavelength long. Dent's interactive coupler 320' is lossy in realization, and has a narrow bandwidth of operation. As such, Dent's implementation is not practical for implementation on a microchip or in a microchip package.

In contrast, the claimed invention uses lumped element impedance inverters. As described in the Application, "Instead of using such a quarter-wave length transmission line, the impedance inversion (transformation) can also be achieved using a lumped element equivalent circuit, as known to persons skilled in the art." (Application, p. 3). These lumped element

impedance inverters have the advantages of being small, having low loss, and having a broad bandwidth of operation. However, in isolation, these elements cannot be manufactured, as they require two negative value inductors that cannot be realized.

The claimed invention incorporates Applicant's realization that, while the lumped element impedance inverter cannot be realized in isolation, it can be realized when the two negative value inductors (at its input and output) are incorporated into adjacent circuits having positive inductors, which are required for other purposes. Thus, the claimed invention comprises at least two steps: (1) designing an ideal lumped element circuit with theoretical negative reactance values attributable to some of the idealized elements, and with the desired overall impedance inversion characteristics, and (2) constructing an actual lumped element circuit, wherein the theoretical negative reactance values have been actually incorporated into other elements throughout the circuit. These steps are illustrated in the figures and text of the present Application.

The specification of this Application further clarifies this process:

> As illustrated by Figure 5, the present invention is achieved by first transforming, by means of an impedance inverter 335 (consisting of series positive inductor 250 and shunt negative inductors 260, 270), the output of a Class F amplifier (i.e. at terminal 333) from that of a low impedance voltage source to a high impedance current source so that such output-transformed amplifier may be connected in parallel with another like amplifier configuration to combine the outputs of the two amplifiers. Then, as illustrated by Figure 6, the parallel third harmonic resonator 330, 340 is transformed through that impedance inverter 335 into a series third harmonic resonator 360, 370 (i.e. the parallel resonator 330,340 is replaced by a series resonator 360, 370 across the output terminal 351 and ground). Then, as illustrated by Figure 7 (which shows two such amplifier circuits 500, 501, each configured in accordance with the present invention and connected in parallel to present an output signal at terminal 550 representing an amplification and combination of input signals Vin1 and Vin2) the negative impedances 260, 270 are eliminated by incorporating those negative impedance values (effects) into the values of pre-selected existing reactive components adjacent to them.
>
> Specifically, as shown by Figure 7, the negative impedance 260 is incorporated into the series second harmonic resonator 310, 320 to form a modified series second harmonic resonator 310a, 320a in the example shown. Alternatively, if the source bias voltage 305 is stable, that negative impedance could be incorporated into the source bias inductor 307. Also as illustrated by Figure 7, the negative impedance 270 is incorporated into the series third harmonic resonator

360, 370 in the example shown to form a modified series third harmonic resonator 360a,370a.

(Application, pp. 8-9).

As illustrated in Figure 6 of the present Application, the theoretical negative inductors 260, 270 have negative values, $-L_{\text{inverters}}$ that must be identical to the positive value inductor 250, L_{inverter}. This value is determined by the inductance available to the designer based on the technology being employed, such as spiral inductors on semiconductor or wire bond inductance.

Also illustrated in Figure 6, at the input to the lumped element impedance inverter is a series resonator circuit consisting of a positive value inductor 310 and a capacitor 320. The purpose of this resonator is to provide zero impedance at the second harmonic of the amplifying device 300, and a predetermined high impedance (high negative reactance) at the fundamental harmonic of the amplifying device 300. One skilled in the art at the time the invention was made would recognize that these two conditions uniquely determine the values of the inductor 310 and capacitor 320. Mathematically, this can be represented as follows:

$$2\,\omega = (L\,C)^{-1/2}$$

And

$$j\,X = -j\,[(1 / \omega\,C) - \omega\,L]$$

Here ω is the fundamental frequency and 2 ω is the second harmonic.

When the resonator consisting of 310, 320 is considered together (in parallel) with the (theoretical) negative value inductor 260, the required zero impedance at the second harmonic remains zero, but the combined high impedance (high negative reactance) at the fundamental harmonic is changed to $-j\,X_{\text{new}}$

$$2\,\omega = (L\,C)^{-1/2}$$

And

$$j\,X_{\text{new}} = j\,(\omega\,L - 1 / \omega\,C)\;||\;(-j\,\omega\,L_{\text{inverter}})$$

$$= -j\,L_{\text{inverter}}\,[\omega^2\,L - 1 / C] / [\omega\,(L - L_{\text{inverter}}) - 1 / \omega\,C)]$$

With a predetermined value for $-L_{inverter}$ there again remains two conditions (zero impedance at the second harmonic 2ω, high negative reactance at the fundamental frequency ω) that can be met with two components, one inductor L, and one capacitor C. Further, the values for L and C will always be positive and hence realizable.

A similar method of incorporating the lumped element impedance inverter output negative value inductor into the third harmonic resonator results in achieving lumped element impedance inversion, input second harmonic resonance and output third harmonic resonance with real positive value inductors and capacitors.

In sum, Applicants assert that the specification fully supports the claims, as amended, and satisfies the written description requirements of 35 U.S.C. §112. In addition, Applicants assert that the claimed invention differs from Dent, in that Dent makes use of a distributed element impedance inverter, while the claimed invention comprises a lumped element impedance inverter.

Applicant believes the above amendments and remarks to be fully responsive to all the objections and grounds of rejection raised by the Examiner. In view of these amendments and remarks, all the claims currently pending in the present patent Application are believed to be in condition for allowance. Prompt notice to this effect is respectfully requested.

Respectfully submitted,

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